Variable Periphery Amplifier With Built-In Phase Shifting Capability for Ultra Compact Transceiver Module

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Abstract- ***The objective of this paper is to provide an novel solution to construct an ultra compact transceiver module to achieve cost saving and weight reduction goals required for a large aperture phased array. The idea is to utilize variable periphery amplifiers to modulate the magnitude of the in-phase and quadrature component of the input signal. The phase of the combined signal then can be varied in a similar fashion to an IQ modulator. The advantage of the approach is the realization of an amplifier with built-in phase shifting capability. The typical performance degradation associated with the phase shifter in the conventional design can then be avoided.***

II. INTRODUCTION

For surveillance applications, it is desired to have a large aperture array since it can produce extremely small beam width to enhance the resolution of the target. However, The cost of the conventional transceiver (T/R) module raises affordability issues for such a system. In this paper, an innovative transceiver MMIC implementation is presented to address the challenges of the large aperture phased array system. The variable periphery amplifier (VPA) will generate a high-performance, ultra compact T/R module with reduced weight and cost to realize such a system.

In conventional T/R MMIC implementation, the size of phase shifter (especially at C and X frequency bands) dominates the overall size of the MMIC which establishes the limit for T/R cell compaction. The proposed approach is to implement an amplifier with built-in phase varying capability to eliminate the need for a phase shifter. Besides the obvious size advantage, there are several other advantages to this approach. For instance, no increase complexity in control lines is required since the control lines for the phase shifter can be re-deployed to control the VPAs. Phase state for the amplifier are direct digital signal controllable since gate of the FET draws nearly no current. This enables simplified integration with the system control network. In addition, the amplifier can also act as a programmable linearizer to provide good AM/AM and AM/PM performance without paying the penalties of degraded efficiency and power consumption while meeting the stringent system requirement.

II. DESIGN AND SIMULATION

In this section, design and simulation results for the variable periphery amplifier will be presented. Figure 1 shows a summary of key amplifier parameters and associated design goals. Note here that since there are overwhelming numbers of transceiver elements, output power of each element need not be great.

Figure 1. Summary of Key Amplifier Parameters and Design Goals.

Modes	Parameters	Design Goals
Amplifier	Bandwidth	1GHz
	P1dB	>10 mW
	DC Power	<50 mW
Phase Shift	No. of Bits	3
	Accuracy	+/- 2 deg.

The basic building block of the VPA is using dual-gate devices of various pre-determined sizes (See Figure 2). Each device in the VPA can be invoked separately as to alter the output of the VPA.

The actual operation of the proposed approach is as follows: The input signal is first separated into an in-phase and quadrature component. The two 90 degree out-of-phase components are then fed into two distinct VPA to vary their signal strength (See Figure 3).

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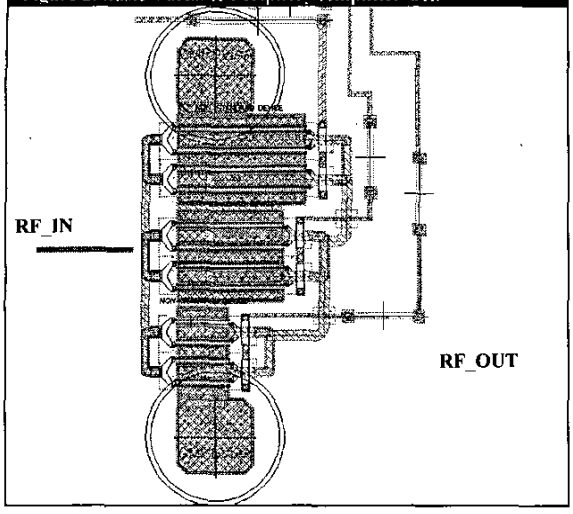
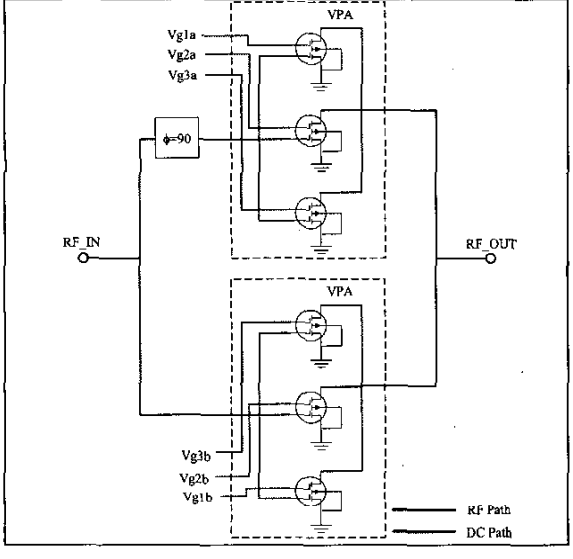
Figure 2. Basic Variable Periphery Amplifier Cell



By direct combine the two resulting signals, one recovers the original signal with added phase shift. In addition, one can minimize amplitude variation by carefully choose the sizes of the devices in the VPA so that the two quadrature components always add up to a constant output power.

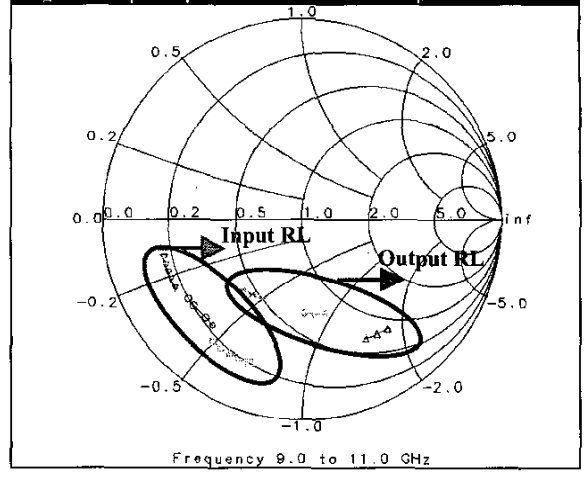
Figure 3. Schematic of the Proposed T/R Cell



To control the impedance variation between phase states, the on/off states of the device are controlled using the second gate so that the first gate can be constantly biased to maintain Cgs and minimize input impedance variation (See Figure 4).

Since the output power is designed to be constant, the equivalent periphery as one looks into the output port will also be constant. Thus, the output impedance variation will also be minimum between phase states.

Figure 4. Input impedance variation between phase States.



Several challenges were encountered during the preliminary design phase. First of all, it was assumed that the gain of the device scales linearly with the periphery. Using conventional transistor linear model, the assumption seems to be valid at low frequencies since common source FET voltage gain is

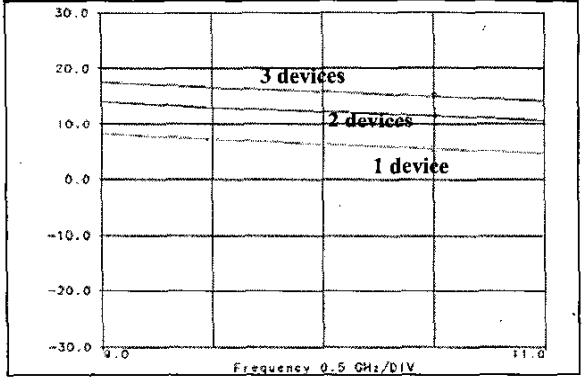
$$gain = -g_m\left(\frac{r_o}{R_d}\right) \qquad (1)$$

where r_o is the intrinsic output resistance, R_d is the external bias drain load resistor, and

$$g_m = kW\left(\frac{V_{gs} - V_t}{L}\right) \qquad (2)$$

Thus, for fixed *Vgs*, g_m is linearly related to *W*, the periphery of the device. It must follow that voltage gain will also be linear related to *W*. Figure 5 shows the validity of our assumption in the frequency band of interest. Three 300 μm dual gate devices with same periphery is turned-on one at a time. Single device shows a gain of about 9 dB. Second device added twice the periphery or 6 dB of power gain. Addition of the third device only adds 3 dB of power gain since only 50% more periphery is added.

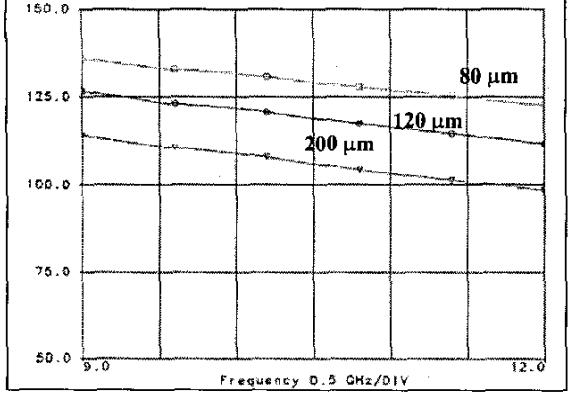
Figure 5. Simulation plot showing linear relationship between gain and periphery looking at magnitude of the S21 in dB.



However, for higher frequency of operation, this relationship may deviate due to parasitic effect. Compensation network needs to be implemented to maintain the linear relationship between voltage gain and device periphery.

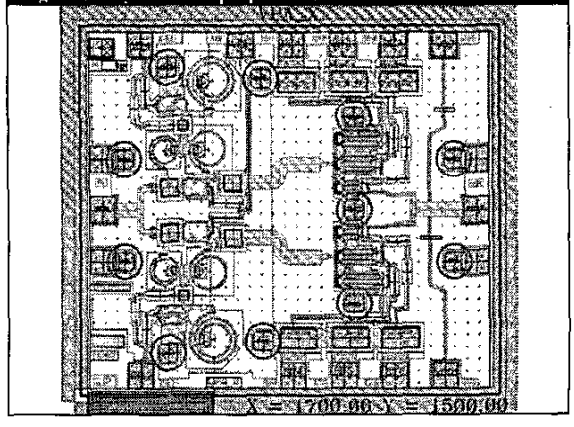
In addition, there are several contributors which can cause phase deviation from the intended design. For instance, the VPA contains several different sizes of devices which have different physical length. As a result, the final combining structure length will need to be added or subtracted to compensate for the difference. Furthermore, the phase progression through the devices also depends highly on the size of the device. Larger devices tend to incur less phase when compared to the smaller devices (See Figure 6).

Figure 6 S21 Phase Variation between different device sizes.



The final layout of the amplifier with optimized combining network is shown in Figure 7. The amplifier include 3-bit phase shifting capability and occupies 2.55 mm^2 area.

Figure 7. Layout of the proposed T/R Cell.



III. MEASUREMENT AND VALIDATION

(To Reviewers: We are currently working on obtaining the measurements for these amplifiers which have just been completed thru processing. Data will be provided with the final manuscript.)

IV. CONCLUSION

We have proposed and plan to demonstrate a novel approach for implementing an amplifier with built-in phase shifting capability. The size and cost of such compact T/R cell will enable the realization of a future large aperture phase array system. We intend to further enhance the maturity of these technologies in support of the vision for future large aperture surveillance systems.